Peter Zhi Xuan Li

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PARTICULARS

EDUCATION

Massachusetts Institute of Technology — Cambridge, MA, United States
Ph.D. in Electrical Engineering & Computer Science — June 2020 - December 2025
Thesis title: *Memory-Efficient 3D Map Construction using Gaussians: Algorithms & Chips*
Supervised by Prof. Vivienne Sze & Sertac Karaman

Massachusetts Institute of Technology — Cambridge, MA, United States
M.Sc. in Electrical Engineering & Computer Science — July 2018 - May 2020
Thesis title: *High-throughput Computation of Shannon Mutual Information on Chip*
Supervised by Prof. Vivienne Sze & Sertac Karaman

University of Toronto — Toronto, ON, Canada
B.A.Sc. in Engineering Science — Sept. 2013 - April 2018
Major in Electrical and Computer Engineering; High Honours; GPA: 3.99/4.00
Thesis title: *Wirelessly-Powered Implantable Chip for Brain Chemistry Monitoring*
Supervised by Prof. Roman Genov, Intelligent Sensory Microsystems Laboratory

RESEARCH INTERESTS

I work on *energy-efficient spatial intelligence*, the embodied AI by which robots perceive, map and act, from one robot to a collaborative team. Because data movement can dominate energy consumption, I pursue *representation co-design*, which widens co-design from algorithms and hardware to spatial representations shared across tasks and robots. These representations determine much of what a robot stores, computes and exchanges. Because AI models generate, interpret and become these representations, their design bridges AI with computer architecture and networked systems. My doctoral work co-designed compact Gaussian maps and a 16 nm chip that builds and queries them in real time under 6 mW of core power. My future research extends representation co-design from efficient computing within a robot to efficient communication across collaborating robots. I will investigate how spatial representations, algorithms, and specialized hardware jointly determine efficiency across these settings. Applications range from homes and offices to species monitoring, domain awareness and planetary exploration.

PUBLICATIONS AND PREPRINTS

* Equal contribution / Co-first authorship

CONFERENCE PAPERS

1. Z. S. Fu*, **P. Z. X. Li***, S. Karaman, V. Sze, "Gleanmer: A 6 mW SoC for Real-Time 3D Gaussian Occupancy Mapping", *IEEE/JSAP Symposium on VLSI Technology and Circuits (VLSI 2026)*, Honolulu, June 2026. **(Best Demo Award)** [Website] [MIT News] [Tech Briefs Interview]

2. **P. Z. X. Li**, S. Karaman, V. Sze, "Memory-Efficient Gaussian Fitting for Depth Images in Real Time", *International Conference on Robotics and Automation (ICRA 2022)*, Philadelphia, May 2022.

3. K. Gupta, **P. Z. X. Li**, S. Karaman, V. Sze, "Efficient Computation of Map-scale Continuous Mutual Information on Chip in Real Time", *International Conference on Intelligent Robots and Systems (IROS 2021)*, Prague, September 2021.

4. **P. Z. X. Li***, Z. Zhang*, S. Karaman, V. Sze, "High-throughput Computation of Shannon Mutual Information on Chip", *Robotics: Science and Systems (RSS 2019)*, Freiburg, June 2019.

5. **P. Z. X. Li**, H. Kassiri, R. Genov, "A Compact Low-Power VLSI Architecture for Real-Time Sleep Stage Classification", *IEEE Int. Symp. on Circuits and Systems (ISCAS 2016)*, Montreal, May 2016.

JOURNAL PAPERS

1. **P. Z. X. Li***, Z. S. Fu*, S. Karaman, V. Sze, "Gleanmer: A 6 mW SoC for Real-Time 3D Gaussian Occupancy Mapping," *Under review.*

2. D. Gao*, **P. Z. X. Li***, V. Sze and S. Karaman, "GEVO: Memory-Efficient Monocular Visual Odometry Using Gaussians," in *IEEE Robotics and Automation Letters*, vol. 10, no. 3, pp. 2774-2781, March 2025, doi: 10.1109/LRA.2025.3534683.

3. **P. Z. X. Li**, S. Karaman and V. Sze, "GMMap: Memory-Efficient Continuous Occupancy Map Using Gaussian Mixture Model," in *IEEE Transactions on Robotics (T-RO)*, vol. 40, pp. 1339-1355, 2024, doi: 10.1109/TRO.2023.3348305.

4. N. Sarhangnejad, N. Katic, Z. Xia, M. Wei, N. Gusev, G. Dutta, R. Gulve, **P. Z. X. Li**, H. Ke, H. Haim, M. Moreno-García, D. Stoppa, K. Kutulakos, R. Genov, "Dual-tap Computational Photography Image Sensor with Per-pixel Pipelined Digital Memory for Intra-frame Coded Multi-exposure", *IEEE Journal of Solid-State Circuits (JSSC)*, 54(11), pp. 3191-3202, November 2019.

GRANTS, FELLOWSHIPS & RECOGNITIONS

Federal Grant Writing Experience

NSF CPS: Medium: Chips for Efficient and Robust Navigation Awarded 2024

- Co-authored the successful technical proposal (PI: Prof. Sertac Karaman; co-PI: Prof. Vivienne Sze) for a **$1,200,000** grant focused on hardware-algorithm co-design for autonomous systems.

Research Fellowships & Awards

RSS Pioneers RSS, 2026
Selected early-career cohort at Robotics: Science and Systems (18% acceptance).

MathWorks Fellowship MIT, 2023
Awarded for memory-efficient algorithm and hardware co-design for 3D mapping.

Qualcomm Innovation Fellowship Finalist MIT, 2023
Algorithm and hardware co-design for enabling robust SLAM on energy-constrained devices.

First Place, Graduate Winner at the ACM SRC Grand Finals ACM, 2020
First prize at the international research competition across the entire ACM.

NSERC Postgraduate Scholarship - Doctoral (PGS-D) NSERC, 2020
Natural Sciences and Engineering Research Council of Canada doctoral scholarship, held at MIT.

First Place, ACM Student Research Competition (SRC) at MICRO-52 SIGMICRO, 2019
Awarded for research that enables real-time autonomous exploration for robots.

EECS Grad Alumni Fellowship MIT, 2018
Awarded to top incoming Ph.D. candidates at MIT EECS.

Governor General's Silver Medal, Nominee University of Toronto, 2018
Nominated by the Faculty of Applied Science and Engineering for exceptional academic performance in an undergraduate degree program.

COMMUNITY LEADERSHIP & SERVICE

Workshop Organization

Co-Organizer, Workshop on Gaussian Representations for Robot Autonomy RSS 2025, June 2025
Organized the inaugural workshop at *Robotics: Science and Systems* (RSS), Los Angeles, with colleagues at CMU and MIT: invited talks, spotlight talks selected from submissions, and posters on challenges and opportunities for Gaussian-based representations in perception and mapping. Also an invited speaker.

Talks

Center for Integrated Circuits and Systems, Cambridge, MA Nov. 2025
"Gleanmer: A 6 mW SoC for Real-Time 3D Gaussian Occupancy Mapping"

Intel University Shuttle Program May 2024
"Extensible SoC Platform and Sensor Debug Interface for Microbots"

Center for Integrated Circuits and Systems, Cambridge, MA Nov. 2023
"GMMap: Memory-Efficient Continuous Occupancy Map Using Gaussian Mixture Model"

Center for Integrated Circuits and Systems, Cambridge, MA Nov. 2019
"A Mutual Information Accelerator for Autonomous Robot Exploration"

MIT College of Computing Launch, Cambridge, MA Feb. 2019
"Efficient Computing for Low Energy Robotics", as one of the EECS department's representatives

Analog Devices Inc., Boston, MA June 2017
"Efficient Layout Techniques in TSMC 16nm FinFET using Tileable Transistors"

Professional Service

Technical Reviewer

Journals: Autonomous Robots (AURO)
Conferences: Robotics: Science and Systems (RSS), IEEE International Conference on Robotics and Automation (ICRA)

Department Service

Course Development, MIT 6.6010 2022 – 2025
In summer 2023, worked with Intel to bring its Intel 16 process to MIT EECS for taping out digital chips. The Fall 2022 and Fall 2025 teaching-assistant terms were beyond my degree's requirement.

TEACHING & MENTORING EXPERIENCES

TEACHING EXPERIENCE

Guest Lecturer, MIT 6.6010 Fall 2026
Analysis and Design of Digital Integrated Circuits

- Lecture: *Interconnect Modeling.*

Graduate Teaching Assistant, MIT 6.6010 Sept. 2025 – Dec. 2025
Analysis and Design of Digital Integrated Circuits

- Delivered lectures to undergraduate and graduate students on *Interconnect Modeling* and *Clock Distribution*.
- Created two *Final Project Infrastructure* tutorial sessions that walk students through the full project flow and tie each part to its course section.

Consulting Teaching Assistant, MIT 6.6010 Summer 2023
Analysis and Design of Digital Integrated Circuits

- Wrote the process-migration document from *SkyWater SKY130* to *Intel 16*, so that the Fall 2023 teaching assistants could update the problem sets.

Graduate Teaching Assistant, MIT 6.6010 Sept. 2022 – Dec. 2022
Analysis and Design of Digital Integrated Circuits

- Redesigned the problem sets to reflect current industry and academic practice in IC design (the co-TA redesigned the digital portion).
- Guided students through analog and digital design flows using the *SkyWater SKY130* process node, which replaced a simplified teaching process.
- Developed a new final project module involving digital synthesis and place-and-route (PnR) for a RISC-V subsystem, with SystemVerilog recitations and a subsystem template for students new to RTL design.

MENTORING EXPERIENCE

Zih-Sing Fu (Currently pursuing a Ph.D.) June 2023 - December 2025
Project: *SoC for Enabling Real-Time 3D Mapping and Localization on Micro-robots*

Sarah Lov (MIT UROP) Sept. 2025 - December 2025
Project: *PCB Design for Real-Time, On-Chip Sensor Data Processing on Low-Power Robots*

Dasong Gao (Currently pursuing a Ph.D.) Sept. 2022 - May 2025
Project: *Memory-Efficient Visual-Inertial Odometry*

Keshav Gupta (MIT SuperUROP, M.Eng.) May 2020 - May 2024
Thesis: *Efficient Computation of Map-scale Continuous Mutual Information on Chip in Real Time*

Adrianna Wojtyna (MIT UROP, M.Eng.) Sept. 2022 - May 2024
Thesis: *Energy-Efficient Real-Time Hardware Acceleration for Gaussian Fitting*

Alex Studer (M.Eng.) Sept. 2023 - May 2024
Thesis: *Extensible Real-Time Sensor and Test Interface for a System-on-a-Chip*

Kailas Kahler (MIT UROP, M.Eng.) Jan. 2023 - May 2025
Project: *FPGA Platform for Prototyping RISC-V Subsystem and Custom Instruction Set*

Ezra Kang (MIT UROP, M.Eng.) June 2023 - May 2025
Project: *Real-Time Operating System Design for System-on-a-Chip on Low-Power Robots*

PROFESSIONAL EXPERIENCE

Embedded Systems Engineer, Tycho AI Inc. Jan. 2026 – Present
Cambridge, MA, United States

- Lead the specialized hardware team and the *hardware-algorithm co-design* of the perception and localization stack for next-generation autonomous drones, increasing real-time throughput at comparable accuracy within power, cost, and latency limits.

- Designed the target-tracking algorithm with *two AI models*, the second running only on regions of interest; in field tests it increased throughput and reduced energy per frame at comparable accuracy.
- Co-design the tracking algorithm with the *sensor resolution* that dictates the detection range.
- Deployed my doctoral *GMMap* for real-time terrain mapping on fast, low-flying drones, and design memory-efficient localization for specialized, resource-constrained hardware.
- Co-design the system for *adoption*, balancing efficiency with affordability, manufacturability, and supply-chain security.

IC Design Intern, Analog Devices Inc. May 2016 – Aug. 2017
Toronto, Canada

- Designed and laid out high-performance analog architectures, including *amplifiers, comparators, and clock distribution paths*.
- Specialized in deep-submicron nodes, utilizing *TSMC 28nm* and *16nm* technologies within the Cadence Virtuoso environment.
- Contributed to the development of commercial-grade ADC products through global collaboration with design centers, ensuring rigorous signal integrity and power standards.